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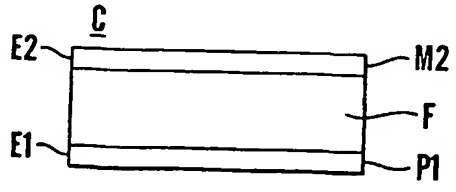
(54) Title: A FERROELECTRIC MEMORY CIRCUIT AND METHOD FOR ITS FABRICATION



(57) Abstract: A ferroelectric memory circuit (C) comprises a ferroelectric memory cell in the form of a ferroelectric polymer thin film (F) and first and second electrodes (E_1; E_2) respectively, contacting the ferroelectric memory cell (F) at opposite surfaces thereof, whereby a polarization state of the cell can be set, switched or detected by applying appropriate voltages to the electrodes (E_1; E_2). At least one of the electrodes (E_1; E_2) comprises at least one contact layer (P_1; P_2), said at least one contact layer (P_1; P_2) comprising a conducting polymer contacting the memory cell (C), and optionally a second layer (M_1; M_2) of a metal film contacting the conducting polymer (P_1; P_2), whereby said at least one of the electrodes (E_1; E_2) either comprises a conducting polymer contact layer (P_1; P_2) only, or a combination of a conducting polymer contact layer (P_1; P_2) and a metal film layer (M_1; M_2). A method in the fabrication of a ferroelectric memory circuit of this kind comprises steps for depositing a first contact layer of conducting polymer thin film on the substrate, depositing subsequently a ferroelectric polymer thin film on the first contact layer, and then depositing a second contact layer on the top of the ferroelectric polymer thin film.

A ferroelectric memory circuit and method for its fabrication

The present invention concerns a ferroelectric memory circuit comprising a ferroelectric memory cell in the form of a ferroelectric polymer thin film and first and second electrodes respectively contacting the ferroelectric the memory cell at opposite surfaces thereof, whereby a polarization state of the cell can be set, switched and detected by applying appropriate voltages to the electrodes. The invention also concerns a method in the fabrication of a ferroelectric memory circuit of this kind, wherein the memory circuit is provided on an insulating substrate.

The present invention deals with the polarization and switching process in a ferroelectric polymer thin film in memory circuits. Such circuits are used to realize bistable ferroelectric memory devices.

In particular the present invention concerns how to improve the performance of ferroelectric poly(vinylidene fluoride-trifluoroethylene) polymer thin and ultrathin films in a circuit of this kind, where memory cells in the thin film are switched between two polarization states by means of an electric field.

Ferroelectric thin (0.1 μm to 1 μm) and ultrathin (below 0.1 μm) films can be used as bistable memory devices are well-known in the prior art. The use of ferroelectric polymer in thin film form can realize fully integrated devices in which polarization switching can occur at low voltages. However, the investigation of the thickness dependence of polarization behaviour of the most widely used ferroelectric polymer according to prior art, i.e. polyvinylidene fluoride-trifluoroethylene (PVDF-TFE), shows that the polarization level decreases and the switching field increases as the thickness is reduced, and further that a large drop in the polarization level is observed as the thickness is reduced to below 100 nm. In PVDF-TFE polymer films, the polarization behaviour is directly related to the crystallinity and crystallite size in the film. It is believed that in thin films, a stiff metal substrate on which the film is normally deposited by spin-coating, may inhibit the crystallization process due to the heterogeneous nucleation process which determines the crystallite orientation being influenced by the substrate. As a result, neighbouring crystallites may have large orientation mismatches which cause a high elastic energy in the film and prevent the further growth of crystallites, thus creating an interface region between the metal substrate and the thin film. On the other hand, recent experimental

results seem to indicate that a high crystallinity may be obtained even with a metal substrate, so that the actual mechanism at present remains somewhat unclear. The interface has a thickness which is a considerable fraction of the thin film thickness, causing a lower polarization level and a higher coercive field. Due to said interface, thin films in contact with a metal layer exhibit a lower polarization level and high switching field.

Hence, a major object of the present invention is to obviate the above-mentioned disadvantages of the prior art technology for ferroelectric memory circuits. Particularly it is also an object of the present invention to improve the polarization and switching behaviour in ferroelectric memory circuits with ferroelectric polymer thin films as the memory material.

The above objects as well as further features and advantages are realized with a ferroelectric memory circuit according to the invention which is characterized in that at least one of the electrodes comprises at least one contact layer, said at least one contact layer comprising a conductive polymer contacting the memory cell, and optionally a second layer of a metal film contacting the conducting polymer, whereby said at least one of the electrodes either comprises a conducting polymer contact layer only, or a combination of a conducting polymer contact layer and a metal film layer.

In an advantages embodiment of the ferroelectric memory circuit of the invention, wherein only one of the electrodes comprises the conducting polymer contact layer, the other electrode comprises a single metal film layer.

Preferably the ferroelectric polymer thin film has a thickness of 1 μm or less and preferably the conducting polymer has a thickness between 20 nm and 100 nm.

Preferably the ferroelectric memory cell comprises at least one polymer selected among one of the following, viz. polyvinylidene fluoride (PVDF), polyvinylidene with any of its copolymers, ter-polymers based on either copolymers or PVDF-trifluoroethylene (PVDF-TFE), odd-numbered nylons, odd-numbered nylons with any of their copolymers, cynopolymers, and cynopolymers with any of their copolymers. In that connection it is preferred the conducting polymer of the contact layer is selected among one of the following, viz. doped polypyrrole (PPy), doped derivatives of polypyrrole

(PPy), doped polyaniline, doped derivatives of polyaniline, doped polythiophenes, and doped derivatives of polythiophenes.

Generally it is preferred that the conducting polymer of the contact layer is selected among one of the following polymers, viz, doped polypyrrole (PPy), doped derivatives of polypyrrole (PPY), doped polyaniline, doped derivatives of polyaniline, doped polythiophenes, and doped derivatives of polythiophenes.

It is also preferable that metal of the metal film layer is selected among one of the following, viz. aluminium, platinum, titanium and copper.

Advantageously the ferroelectric memory circuit according to the invention forms a memory circuit in a matrix-addressable array of similar circuits, that memory cell of a memory circuit forms a portion in a global layer of ferroelectric polymer thin film, and the first and second electrodes form portions of a first and second electrode means respectively, each electrode means comprising a plurality of parallel strip-like electrodes with the electrodes of the second electrode means being oriented at an angle, preferably orthogonally, to the electrodes of the first electrode means with the ferroelectric polymer thin film global layer in sandwich therebetween, such that the ferroelectric memory cell is defined in the ferroelectric polymer thin film at the crossings of respectively the electrodes of the first electrode means and the electrodes of the second electrode means, whereby the array formed by the electrode means and the ferroelectric polymer thin film with the memory cells forms an integrated passive matrix-addressable ferroelectric memory device wherein the addressing of respective memory cells for write and read operations take place via the electrodes of the electrodes means in a suitable connection with external circuitry for driving, control and detection.

The above-mentioned objects as well as further features and advantages are also realized with a method in the fabrication of ferroelectric memory circuit according to the invention, the method being characterized by depositing a contact layer of conducting polymer on the substrate, depositing subsequently a ferroelectric polymer thin film on the contact layer, and then depositing a second contact layer on the top of the ferroelectric polymer thin film.

In the method according to the invention it is considered advantageous depositing a metal film layer on the substrate before the first contact layer is deposited and depositing the latter subsequently.

In the method according to the invention it is preferable depositing the conducting polymer thin film by means of spin coating, and similarly depositing the ferroelectric polymer thin film on the first contact layer by means of spin coating.

In a preferred embodiment of the method according to the invention the first contact layer and/or the ferroelectric polymer thin film are annealed at a temperature of about 140°C after the respective deposition steps.

In another preferred embodiment of the method according to the invention a second contact layer of a conducting polymer thin film is deposited on the top of the ferroelectric polymer thin film. In that connection it is preferred to anneal the second contact layer at a temperature of about 140°C without annealing the ferroelectric polymer thin film before depositing the second contact layer, and preferably a metal film layer can be deposited on the top of the second contact layer.

The invention shall be explained in more detail in the following in connection with discussions of exemplary embodiments and examples, with reference to the appended drawing figures in which

fig. 1 shows a ferroelectric memory cell according to prior art,

fig. 2a a first embodiment of a ferroelectric memory cell according to the present invention, fig. 2b second embodiment of a ferroelectric memory cell according to the present invention, fig. 2c a third embodiment of a ferroelectric memory cell according to the present invention, fig. 2d fourth embodiment of a ferroelectric memory cell according to the present invention, fig. 2e a fifth embodiment of a ferroelectric memory cell according to the present invention, fig. 3 schematically a plan view of a ferroelectric memory device as known in the prior art, but with memory circuits according to the present invention,

fig. 4a a section taken along the line X - X in fig.3,

fig. 4b a detail of a memory circuit according to the present invention and as used in the memory device in fig. 3,

fig. 5 a comparison of the hysteresis loop obtained respectively with the memory circuit according to the present invention and a prior art memory circuit, and

fig. 6 the fatigue behaviour of memory circuit according to the present invention compared with that of a prior art memory circuit.

Now various embodiments of the memory circuit according to the present invention shall be discussed, taking a prior art memory circuit as shown in fig. 1 as the point of departure. In fig.1 which shows on section through a prior art memory circuit, a layer F of a ferroelectric thin film polymer is sandwiched between first and second electrodes E_1;E_2 respectively. The electrodes are provided as metal films M_1;M_2 and it is to be understood that the metal of the electrodes may be the same, but not necessarily so.

A first embodiment of a memory circuit C according to the invention as shown in fig. 2a which is similar to the prior art memory circuit in fig. 1, but in the bottom electrode E_1 the metal film M_1 has now been replaced by a thin film P_1 of conducting polymer, while the top electrode E_2 is retained as a metal film electrode.

A second embodiment of the memory circuit C according to the invention shown in fig. 2b and herein both electrodes E_1; E_2 are realized as thin films P_1;P_2 of conducting polymer which in either case can be the same or different conducting polymers.

Fig. 2c shows a third embodiment of the memory circuit C according to the invention and here the first electrode E_1 comprises a conducting polymer thin film P_1 as a contact layer interfacing the ferroelectric polymer F. On the conducting polymer thin film P_1 there is provided a metal film M_1 such that the first electrode E_1 in this case is a composite formed by two layers M_1, P_1. The second electrode E_2 is similar to that of the first embodiment, comprising a metal film M_2 interfacing the ferroelectric thin film polymer F which constitutes the memory material, in other word the memory cell proper.

A fourth embodiment of the memory cell according to the invention is shown in fig. 2d and it differs from the embodiment in fig. 2c in that the second electrode E_2 now comprises a contact layer of conducting polymer thin film P_2 only.

Finally a fifth embodiment of the memory circuit according to the invention is shown in fig. 2e, and here both electrodes E_1; E_2 are now composite, formed of respectively metal film M_1; M_2 and thin film conductor polymer P_1; P_2 provided as a contact layer between the metal film M_1;M_2 and interfacing the ferroelectric thin film polymer F of the memory cell proper.

Conventionally, as known to persons skilled in the art, the prior art memory cell can be applied as a memory cell in a passive matrix-addressable ferroelectric memory device of the kind shown in fig. 3, wherein the memory material, i.e. the ferroelectric thin film, is provided as a global layer G. However, a passive matrix ferroelectric memory device with a similar layer G can also incorporate any of the memory circuit embodiments in figs.2a-2e. A memory device then comprises the ferroelectric thin film polymer provided in a global layer G and used as a memory material in a memory circuit C. Further the memory device comprises first electrode means in the form of strip-like parallel bottom electrodes E_1 interfacing the global layer G of ferroelectric thin film polymer. A second electrode means of similar electrodes E_2 is now provided on the top of the ferroelectric thin film polymer, but with the strip-like parallel electrodes E_2 oriented at an angle, preferably perpendicularly to the electrodes E_1 of the first electrode means. Fig. 4a shows a cross section of the passive matrix-addressable memory device in fig. 3 taken along the line X-X thereof. As rendered the ferroelectric memory device is now provided with a memory circuit C corresponding to the embodiment shown in fig. 2c or fig. 2d, that is with a composite bottom electrode E_1 of a metal film M_1 and a contact layer of conducting polymer P_1 interfacing a portion F the global layer G of ferroelectric polymer thin film used as the memory material in the memory cell.

In the memory device shown in fig. 3 and fig. 4a the overlapping crossing of an electrode E_2 of the second electrode means with an electrode E_1 of the first electrode means defines a memory cell F in the volume of the ferroelectric polymer thin film therebetween as indicated in respectively figs. 3 and 4a. Hence the memory circuit C according to the invention forms a portion of the complete memory array with the ferroelectric memory material F and the electrodes E_1; E_2 as depicted in figs. 3, 4a, although now the electrodes E_1;E_2 of the memory circuit as well as the memory material F thereof, all form respective definable portions of the electrodes E_1; E_2 and the

memory material F as applied globally in the ferroelectric memory device of fig. 3.

Fig. 4b details a memory circuit C as used in a passive matrix-addressable ferroelectric memory device, as emphasized in either fig. 3 or fig. 4a. It will be seen that the memory circuit C in this case corresponds to either the embodiment in fig. 2c or the embodiment in fig. 2d. In other words, while the bottom electrodes E_1 comprises a metal film M_1 and a contact layer of a conductive polymer P_1. The top electrode E_2 may now either be a metal film M_2 or a conductive polymer P_2. There is of course, nothing to preclude the use of any of the embodiments depicted in fig. 2a-2e in the matrix-addressable memory device shown in either fig. 3 and fig. 4a.

Now the present invention shall be discussed in general terms. A memory circuit C according to the invention comprises a ferroelectric polymer thin film on a substrates that is covered with a conductive polymer. According to an aspect of the invention, a soft conducting polymer, such a conducting polythiophene, is deposited onto a metallized substrate, for instance a silicon wafer covered with platinum or aluminum. A ferroelectric thin polymer film, the thickness of which may be 20 nm to 1μm, for instance of polyvinylidene fluoride-trifluoroethylene copolymer (PVDF-TFE) is then deposited on the substrate by e.g. spin-coating. The conducting polymer is used as the bottom electrode, which replaces conventionally used metal electrodes, for instance of metals such as Al, Pt, Au and the like. Provided according to the method of the present invention, the conducting polymer electrodes is thought to increase the crystallinity in the ferroelectric polymer thin film and hence increase the polarization level and reduce the switching field as compared with corresponding thin films on metal electrodes.

The introduction of a conducting polymer as an electrode in the memory cell of the invention serves to reduce the film stiffness, (i.e. increase the film crystallinity) and also to modify the interface electric barrier. Generally, phase separation between polymers reduces a crystal region near their interface. This property is used in the invention by first applying a conducting polymer film on a substrate for forming a bottom electrode. The ferroelectric thin film and the conducting polymer film has a good separation of phase, which will diminish the non-crystallized region of the ferroelectric thin film during a subsequent annealing process. Because of the different

charge conduction mechanism in conducting copolymers compared with metal, it is believed that the interface barrier between the electrode and the ferroelectric polymer film is modified in a manner causing both the polarization level and switching speed in the ferroelectric polymer film to increase, while the switching field is reduced, as actually observed in experiments.

In the present invention, the conducting polymers that may be used include, but are not limited to doped polypyrrole (PPy) and their doped derivatives, doped polyaniline and their doped derivatives, and doped polythiophenes and their doped derivatives.

Ferroelectric polymers that may be used in the invention include, but are not limited to, polyvinylidene fluoride (PVDF) and its copolymers with trifluoroethylene (PVRF-TFE), ter-polymers based on either copolymers or PVDF-TFE, other ferroelectric polymers such as odd-numbered nylons or cynopolymers.

In the present invention, the use of a conducting polymer electrode increases the crystallinity in a PVDF-TFE copolymer thin film are compared with the thin films interfacing electrodes metal, such as Al, Pt, Au and the like. The polarization hysteresis loop show that PVDF-TFE copolymer thin films provided on a conducting polymer electrode have a higher polarization level than those provided with metal electrode, for instance of titanium, under the same applied electric field as shown in fig. 5 which shall be discussed below. The fabrication of thin and ultrathin ferroelectric polymer films on a planar substrate covered with a conducting polymer shall be described in the following examples.

The disclosed embodiments of the invention are presented for purposes of elucidation and not limitation. The examples are not intended, nor are they to be construed as limiting the scope of the disclosure or the claims.

Example 1

In this example a conductive polymer called PEDOT (poly (3,4-ethylene dioxythiophene)) shall be used as one of the electrodes of a ferroelectric polymer in memory circuit with thin film. A PEDOT film can be produced either by chemical polymerization, by electrochemical polymerization or by spin-coating a ready-made solution containing PEDOT-PSS (where PSS is

polystyrene sulphonate). Here, the chemical method of producing a PEDOT film has been used. The solution for preparing such a film is a mixture between Baytron M (3,4-ethylene dioxythiophene EDOT) and Baytron C (ferric toluene sulphonate solution in n-butanol, 40 %), both of them commercially available. The ratio between Baytron C and Baytron M is 6 in the standard mixture solution. Polymerization of EDOT to PEDOT appears around 15 minutes after mixing the two solutions.

The conducting PEDOT polymer is in this example spin-coated on a metallized Si wafer. For polymerization purposes the film is then put on a hot (100 °C) plate for 1 to 2 minutes. A solution washing process follows to remove any non-polymerized EDOT and ferric solution. Isopropanol and deionized water may be alternatively used in this process. On top of the conductive PEDOT film a ferroelectric thin film, in this case 80 nm thick, is deposited by means of spin-coating technique, whereupon an annealing step at 145 °C for 10 minutes follows. A top electrode of titanium is applied to the ferroelectric film by means of evaporation. The ferroelectric film, in this example, is 75/25 copolymer PVDF-TFE.

Fig. 5 shows the hysteresis loop 1 for the ferroelectric polymer thin film processed according to the example 1 disclosed above. The memory circuit C is then provided with a bottom electrode E_1 of PEDOT conducting polymer and with titanium as a top electrode E_2.

Example 2

A conductive polymer, in this case polypyrrole, is deposited on a metallized substrate (such as a silicon wafer covered with Pt or Al) in a known process wherein the substrate is dipped in a solution of the polymer. According to this example, the substrates are dipped into a low concentration polymer solution to reduce the deposition speed. Generally, the substrates may be immersed in the polymerizing solution for about 3 to about 30 minutes at room temperature. A multi-step dipping process may be used to obtain the desired thickness. In the example, a 30 nm final thickness is used for the polypyrrole layer, although the thickness may be varied in the range of 20 nm to about 100 nm by varying the total dipping time. The described step is then followed by a deposition procedure step, wherein the conducting polymer layer is spin-coated with the ferroelectric polymer thin film layer.

In the present example random PVDF-TFE copolymers of 75/25 and 68/32 molar content ratio of VDF/TFE having average molecular weights around 200000 are used for forming the thin film layer. The films are subsequently annealed at 140 °C for 2 hours and cooled slowly down to room temperature.

Example 3

A conducting polymer electrode layer is deposited on a metallized substrate (i.e. a silicon wafer covered with platinum, titanium or aluminum films) or on top of a ferroelectric thin film by spin coating from Baytron P solution. The commercial Baytron P is a waterborn solution of PEDOT in presence of polystyrene sulfonic acid (PSS) which serves as a colloid stabilizer. Due to the poor wetting properties of any of the said metal films and a ferroelectric film, a certain amount of surfactant must be added in the Baytron P to allow a uniform and smooth PEDOT-PSS film formation. After spin coating, a heat treatment at 100°C for 2 –10 minutes is necessary. This process can increase the conductivity of PEDOT/PSS.

A suitable solvent is used for dissolving the ferroelectric polymer. The only requirement is that this solvent shall not dissolve or swell PEDOT-PSS film at room temperature and prevents a possible diffusion process between the ferroelectric thin film and the PEDOT-PSS film. The concentration of ferroelectric polymer in DEC is 3%. To obtain a 90 nm thick ferroelectric film a, spin speed of 3800 rpm is used.

A second PEDOT-PSS conducting polymer layer is formed on top of the ferroelectric polymer film. On top of this second conductive layer an electrode layer of titanium is deposited. This is done by evaporating a 150 nm thick titanium film on top of the conducting polymer. The active area is defined by a shadow mask.

Fig. 5 shows the hysteresis loop that can be obtained with a memory circuit according to the present invention. This memory circuit C essentially corresponds to the embodiment of the memory circuit C in fig 2a and example 1. For the bottom electrode E_1 the conducting polymer P_1 is C-PEDOT, that is polythiophene doped with ferric toluene sulphonate. It is supposed to have higher conductivity than PEDOT-PSS. The top electrode E_2 is made of a titanium metal film. Loop 1 is the hysteresis loop of the memory circuit C according to the present invention, while loop 2 is the hysteresis loop of a prior art memory circuit C with top and bottom electrodes E_1;E_2

both made of titanium. As will be seen, the memory circuit C according to the present invention shows a much higher polarization than the prior art memory circuit, as evident from the compared hysteresis loops. Also the switching polarization $\hat{P}_1$ of the memory circuit C according to the present invention is considerably smaller than the switching polarisation $\hat{P}_2$ of the prior art memory circuit. It should however be noted that the coercive voltage V_c is somewhat higher for the memory circuit of the present invention, probably due to a somewhat larger thickness of the ferroelectric polymer thin film than expected. However, the hysteresis loops compared in fig. 5 clearly shows that the use of bottom electrodes with a conducting polymer, in this case C-PEDOT, improves the polarization of the ferroelectric thin film polymer used as the memory material appreciably.

Fig. 6 compares the fatigue of the memory circuit C according to the present invention with the fatigue of a prior art memory circuit at room temperature. It will be seen that the memory circuit according to the invention shows a much-improved polarization as well as fatigue behaviour and the difference between the memory circuit according to the present invention and the prior art memory circuit is appreciable up to more than 10^6 fatigue cycles.

It is believed that a metal substrate may impose a high elastic energy in ferroelectric thin and ultrathin films due to the orientation mismatch between the neighbouring crystallites which are dictated by using a metal substrate for the ferroelectric polymer thin films. This results in a low crystallinity in ultrathin PVDF-TFE films. As a consequence, ultrathin PVDF-TFE copolymer films of this kind exhibit a lower remanent polarization level and higher switching polarization. In addition, the interface barrier between a metal electrode and ferroelectric polymer film may also increase the switching polarization. In the present invention, the ferroelectric properties of PVDF-TFE films with thickness from 0.05 to 1 μm are characterized. The switching speed under different electric fields has been measured. The experimental results show that, using conducting polymer electrodes, the crystallinity and polarization level are increased due to their match of elastic modulus with that of the ferroelectric polymer films. This is a clear indication that conducting polymer electrodes function properly in ferroelectric thin film devices. Furthermore, it is reasonable to suppose that the modification of the electrode-polymer interface also results in a

beneficial modification of the interface barrier causing both the polarization level and switching speed to increase. More important, the polarization level is higher and the coercive field or voltage lower compared with corresponding results for ferroelectric polymer thin films with metal electrodes under the same experimental conditions..

CLAIMS

1. A ferroelectric memory circuit (C) comprising a ferroelectric memory cell in the form of a ferroelectric polymer thin film (F) and first and second electrodes (E_1;E_2) respectively, contacting the ferroelectric memory cell (F) at opposite surfaces thereof, whereby a polarization state of the cell can be set, switched or detected by applying appropriate voltages to the electrodes (E_1;E_2),
characterized in that at least one of the electrodes (E_1;E_2) comprises at least one contact layer (P_1;P_2), said at least one contact layer (P_1;P_2) comprising a conducting polymer contacting the memory cell (C), and optionally a second layer (M_1;M_2) of a metal film contacting the conducting polymer (P_1;P_2), whereby said at least one of the electrodes (E_1;E_2) either comprises a conducting polymer contact layer (P_1; P_2) only, or a combination of a conducting polymer contact layer (P_1;P_2) and a metal film layer (M_1;M_2).

2. A ferroelectric memory circuit (C) according to claim 1, wherein only one of the electrodes (E_1;E_2) comprises the conducting polymer contact layer (P_1;P_2),
characterized in that the other electrode (E_2;E_1) comprises a single metal film layer (M_2;M_1) only.

3. A ferroelectric memory circuit (C) according to claim 1,
characterized in that the ferroelectric polymer thin film (F) has a thickness of 1 μm or less.

4. A ferroelectric memory circuit (C) according to claim 1, characterized in that the conducting polymer has a thickness between 20 nm and 100 nm.

5. A ferroelectric memory circuit (C) according to claim 1, characterized in that the ferroelectric memory cell (F) comprises at least one polymer selected among one of the following, viz. polyvinylidene fluoride (PVDF), polyvinylidene with any of its copolymers, ter-polymers based on either copolymers or PVDF-trifluoroethylene (PVDF-TFE), odd-numbered nylons, odd-numbered nylons with any of their copolymers, cynopolymers, and cynopolymers with any of their copolymers.

6. A ferroelectric memory circuit (C) according to claim 5, characterized in that the conducting polymer of the contact layer (P) is selected among one of the following, viz. doped polypyrrole (PPy), doped derivatives of

polyoyrrole (PPy), doped polyaniline, doped derivatives of polyaniline, doped polythiophenes, and doped derivatives of polythiophenes.

7. A ferroelectric memory circuit (C) according to claim 1, characterized in that the conducting polymer of the contact layer (P) is selected among one of the following polymers, viz, doped polypyrrole (PPy), doped derivatives of polypyrrole (PPY), doped polyaniline, doped derivatives of polyaniline, doped polythiophenes, and doped derivatives of polythiophenes.

8. A ferroelectric memory circuit (C) according to claim 1, characterized in that the metal of the metal film layer (M) is selected among one of the following, viz. aluminium, platinum, titanium and copper

9. A ferroelectric memory circuit (C) according to claim 1, characterized in that the ferroelectric memory circuit (C) forms a memory circuit in a matrix-addressable array of similar circuits, that the memory cell (F) of a memory circuit (C) forms a portion in a global layer (G) of ferroelectric polymer thin film, and that first and second electrodes (E_1;E_2) form portions of a first and second electrode means respectively, each electrode means comprising a plurality of parallel strip-like electrodes (E_1;E_2) with the electrodes (E_2) of the second electrode means being oriented at an angle, preferably orthogonally, to the electrodes (E_1) of the first electrode means with the ferroelectric polymer thin film global layer (G) in sandwich therebetween, such that the ferroelectric memory cell (F) is defined in the ferroelectric polymer thin film at the crossings of respectively the electrodes (E_1) of the first electrode means and the electrodes (E_2) of the second electrode means, whereby the array formed by the electrode means and the ferroelectric polymer thin film with the memory cells (F) forms an integrated passive matrix-addressable ferroelectric memory device wherein the addressing of respective memory cells (F) for write and read operations take place via the electrodes (E_1;E_2) of the electrodes means in a suitable connection with external circuitry for driving, control and detection.

10. A method in the fabrication of a ferroelectric memory circuit (C), wherein the memory circuit (C) comprises a ferroelectric memory cell (F) in the form of a ferroelectric polymer thin film and first and second electrodes (E_1;E_2) respectively contacting the ferroelectric memory cell (F) at opposite surfaces thereof, whereby a polarization state of the cell can be set, switched or detected by applying appropriate voltages to the electrodes (E_1;E_2) and

wherein the memory circuit (C) is provided on an insulating substrate (S), characterized by depositing a first contact layer of conducting polymer thin film on the substrate, depositing subsequently a ferroelectric polymer thin film on the first contact layer, and then depositing a second contact layer on the top of the ferroelectric polymer thin film.

11. A method according to claim 10, characterized by depositing a metal film layer on the substrate before the first contact layer is deposited and depositing the latter subsequently.

12. A method according to claim 10, characterized by depositing the conducting polymer thin film by means of spin coating.

13. A method according to claim 10, characterized by depositing the ferroelectric polymer thin film on the first contact layer by means of spin coating.

14. A method according to claim 10, characterized by annealing the first contact layer and/or the ferroelectric polymer thin film at a temperature of about 140°C after the respective deposition steps.

15. A method according to claim 10, characterized by depositing a second contact layer of a conducting polymer thin film on the top of the ferroelectric polymer thin film.

16. A method according to claim 15, characterized by annealing the second contact layer at a temperature of about 140°C without annealing the ferroelectric polymer thin film before depositing the second contact layer.

17. A method according to claim 15, characterized by depositing a metal film layer on the top of the second contact layer.

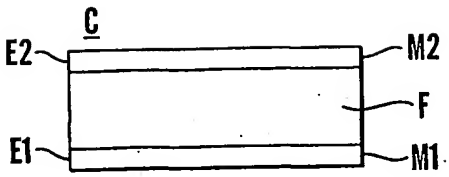


Fig.1 (Prior Art)

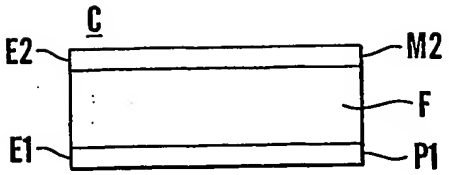


Fig.2a

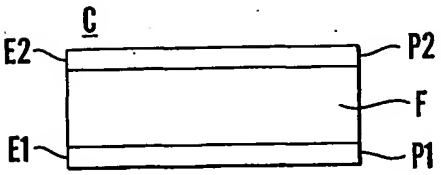


Fig.2b

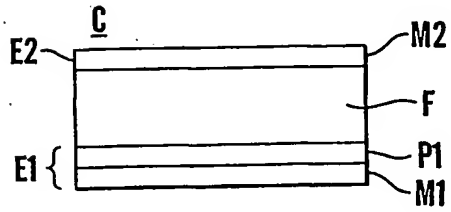


Fig.2c

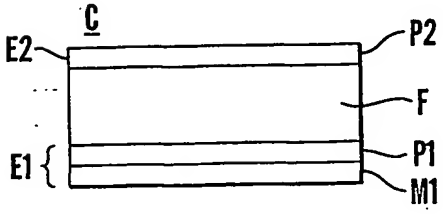


Fig.2d

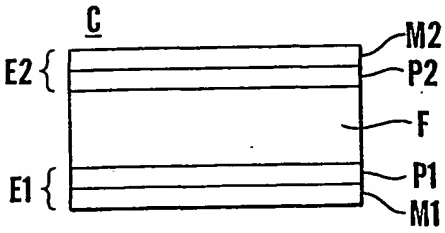


Fig.2e

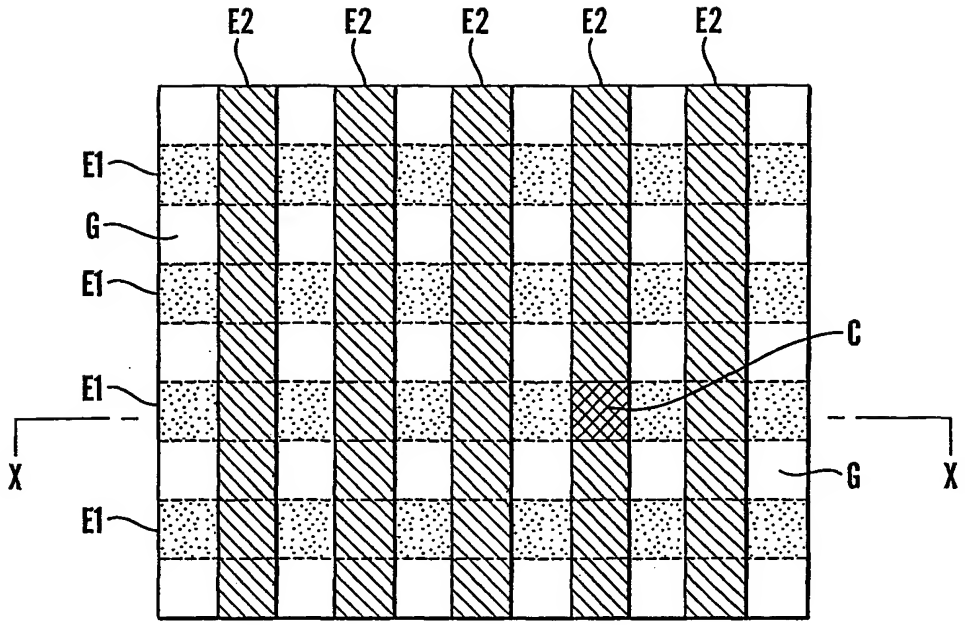


Fig.3

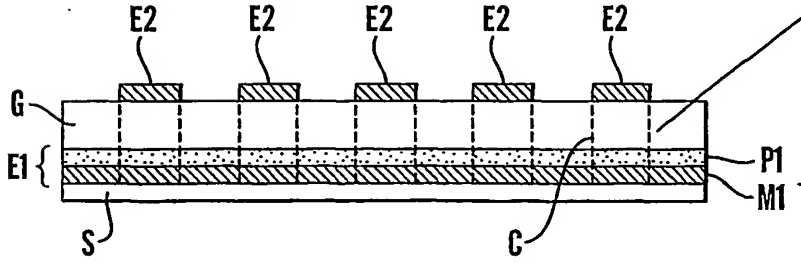


Fig.4a

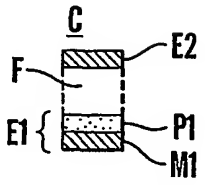


Fig.4b

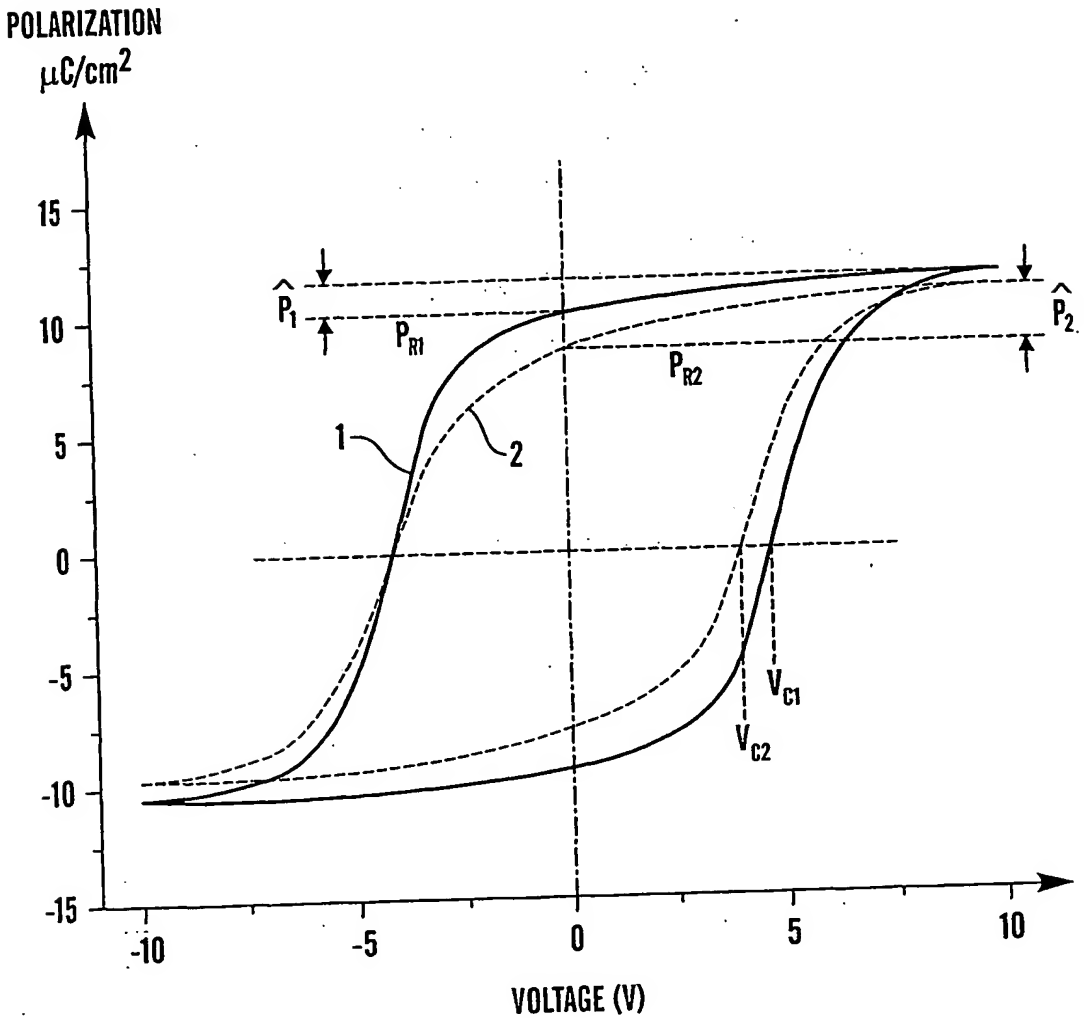


Fig.5

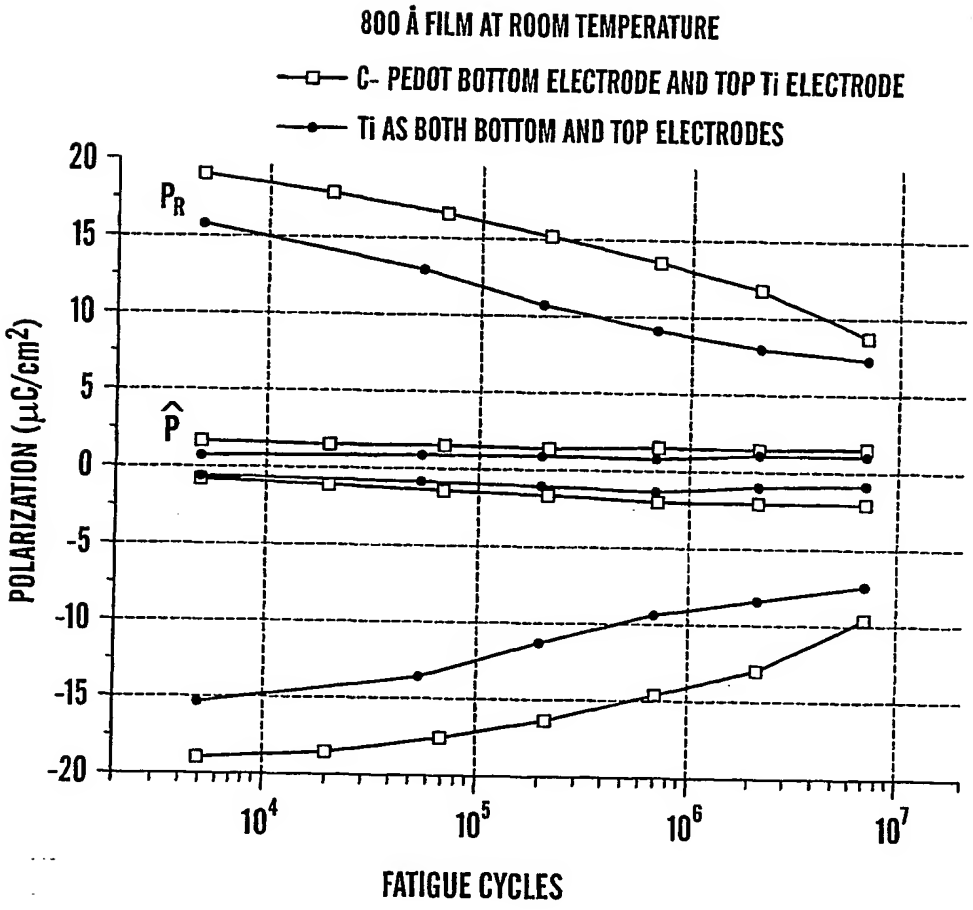


Fig.6

INTERNATIONAL SEARCH REPORT

International application No.
PCT/NO 01/00473

A. CLASSIFICATION OF SUBJECT MATTER

IPC7: G11C 11/22, H01L 21/768, H01L 23/532
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC7: G11C, H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

SE,DK,FI,NO classes as above

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 9858383 A2 (OPTICOM ASA), 23 December 1998 (23.12.98), page 7, line 15 - line 16; page 12, line 12 - line 15; page 19, line 11 - page 20, line 8	1-3,7-9
Y	--	5,6
Y	WO 9814989 A1 (SIEMENS AKTIENGESELLSCHAFT), 9 April 1998 (09.04.98), page 3, line 18 - line 31	5,6
	--	

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier application or patent but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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"Y" document of particular relevance: the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
27 February 2002	07 -03- 2002
Name and mailing address of the ISA/ Swedish Patent Office Box 5055, S-102 42 STOCKHOLM Facsimile No. +46 8 666 02 86	Authorized officer Bo Gustavsson /OGU Telephone No. +46 8 782 25 00

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

Information on patent family members

28/01/02

International application No.
PCT/NO 01/00473

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9858383 A2	23/12/98	AU 735299 B	05/07/01
		AU 8359698 A	04/01/99
		CN 1267389 T	20/09/00
		EP 0990235 A	05/04/00
		JP 2001503183 T	06/03/01
		NO 311119 B	08/10/01
		NO 972803 D	00/00/00
		NO 990617 A	10/02/99
		US 6055180 A	25/04/00
WO 9814989 A1	09/04/98	DE 19640239 A	02/04/98

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